AMENDMENT

In the Specification

Please amend the paragraph on page 3, lines 19-25, as shown below.

In the current invention, a common time-multiplexed bus is used to connect all system components. However, instead of using one timeslot to transfer data just between two nodes, the resultant data from all nodes is transferred in a single timeslot. To do this, all nodes are enabled at the same timeslot. The previous timeslot is used to transfer the value of the grant signal to all nodes. Then during the enabled timeslot the node that is granted the bus will drive data onto the bus and all other nodes will float the bus. This allows the transfer to be done within one timeslot.

Please amend the paragraph on page 9, lines 16-30, as shown below.

In each combinatorial circuit, the ENABLE signal, the TIMESLOT signal, the DATUM signal and the SYSCLK (low) signal are combined in an AND function represented by AND gates 18 and 20. For a given TIMESLOT, the gating signal to the tri-state buffer will be true only if the ENABLE and DATUM signals are true. If this is the case, the active-datum "0" on the input of the tri-state buffer will be gated onto the wired-OR junction 16. Since this junction has previously been precharged to a "1" by pre-charge transistor 30, it will stay high (which represents a "0" in active-low logic) if none of the tri-state buffers is enabled. However, if one or more of the tri-state buffers is enabled, then junction 16 will be driven to a low level (which represents a "1" in active-low logic), thus correctly performing the OR function of the distributed multiplexer. Since the data at junction 16 is active-low, the receiver of the data must reinvert that data to correctly reproduce the distributed multiplexer's output. Alternatively, junction 16 could be implemented in active-high logic, in which case the pre-charge would be to a low level and the input to the tri-state buffer would be a "1." In this case, no inverter is ~~need~~ needed at the receiver.